| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/731,667 | LAMBERT, RUSSELL H. | |
| | Examiner | Art Unit | |
| | Brian Young | 2819 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 3/11/05*.

2. ☒ The allowed claim(s) is/are *35-54*.

3. ☒ The drawings filed on *09 December 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. Claims 35-54 are allowed.

2. The following is an examiner's statement of reasons for allowance: an analog-to-digital-converter (ADC) that converts an analog signal to digital data includes a modulator, a decimation filter, and a time dither clock reduction circuit. The modulator receives the analog signal and a feedback signal and produces a modulated signal at a modulator clock rate. The decimation filter coupled to the modulator, receives the modulated signal, and decimates and filters the modulated signal to produce the digital data. The time dither clock reduction circuit receives the modulated signal and provides the feedback signal to the modulator the time dither clock reduction circuit and applies both clock reduction and time dithering to the modulated signal to produce the feedback signal. This combination of features has not been shown in the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bartz, et al discloses a technique for correcting settling, feed thru, and higher order error mechanisms in a dithered analog-to-digital conversion circuit is disclosed. For each conversion cycle of an ADC, a dither signal is generated by converting a current dither value from a sequence of dither values and is then added to an analog input signal. The ADC converts the analog input signal and dither signal, and the current dither value subtracted, to form a digital output signal. Correction signals

proportional to dither values, which precede or follow the current dither value in the sequence are also generated each conversion cycle and subtracted from the analog input signal. The proportions used to produce the correction signals are adjusted dynamically according to the amount of correlation between the digital output signal and the dither values used to form the correction signals. The correction signals are thereby made to equal the amount of error contributed by a corresponding one of the error mechanisms.

Lambert discloses an Analog-to-Digital-Converter (ADC) that converts an analog signal to digital data. The ADC includes a modulator, a decimation filter, and a time dither clock reduction circuit. The modulator receives the analog signal and a feedback signal and, based there upon, produces a modulated signal at a modulator clock rate. The decimation filter couples to the modulator, receives the modulated signal, and decimates and filters the modulated signal to produce the digital data. The time dither clock reduction circuit receives the modulated signal and provides the feedback signal to the modulator. The time dither clock reduction circuit applies both clock reduction and time dithering to the modulated signal to produce the feedback signal. At each modulator clock cycle, the time dithering clock reduction circuit considers modulated signals for a dithering factor, N, previous modulator clock cycles and a modulated signal for a current modulator clock cycle. If at least one constraint is satisfied for the N previous modulator clock cycles, the time dithering clock reduction circuit is allowed to transition the feedback signal with the modulated signal. If not, the time dithering clock reduction circuit holds the prior value of the feedback signal.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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